1- **For the circuit shown in fig.1&2**

a) Determine the critical frequencies associated with the low-frequency response of the amplifier.
b) Determine the critical frequencies associated with the high-frequency response of the amplifier
c) Which is the dominant critical frequency and Sketch the Bode plot.
d) Determine the voltage gain of the amplifier at one-tenth of the dominant critical frequency, at the dominant critical frequency, and at ten times the dominant critical frequency for the low-frequency response.
e) Determine the phase shift at each of the frequencies used in d.
f) What is the bandwidth of the amplifier.

2- **For the circuit shown in fig.3**

a) Determine the lower critical frequencies. Assume that the load is another identical amplifier with the same R_{in}. The datasheet shows I_{GSS} 100 nA at V_{GS}=-12 V.
b) Find the upper critical frequency for the FET amplifier where C_{iss} =8 pF,C_{rss} =3 pF, and g_m=6500mS

3- **In a certain two-stage amplifier**, the lower critical frequencies are $f_{cl(1)}$=125 Hz and $f_{cl(2)}$= 125 Hz, and the upper critical frequencies are $f_{cu(1)}$=3 MHz and $f_{cu(2)}$=2.5 MHz Determine the bandwidth.

4- What is the dominant lower critical frequency of a three-stage amplifier in which f_{cl}=50 Hz for each stage.

5- f_T=200 MHz is taken from the datasheet of a transistor used in a certain amplifier. If the midrange gain is determined to be 38 and if f_{cl} is low enough to be neglected compared to f_{cu}, what bandwidth would you expect? What value of f_{cu} would you expect?

Assignment Design CE amplifier has a voltage gain of 100 and bandwidth of 1 MHz, maximum power consumption accepted is 50 mW from 12 V DC supply.

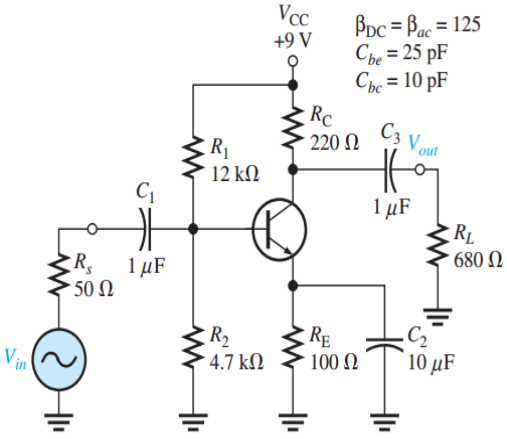

Figure 1

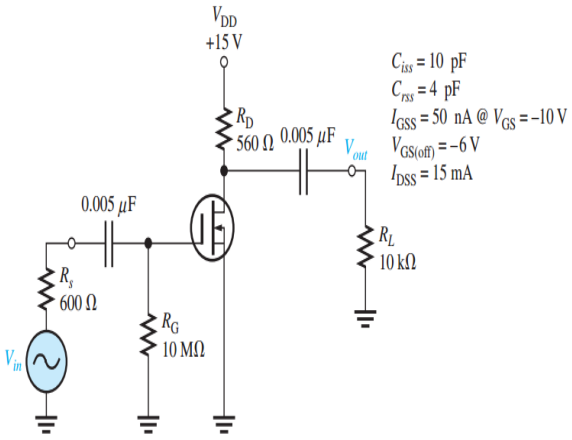

Figure 2

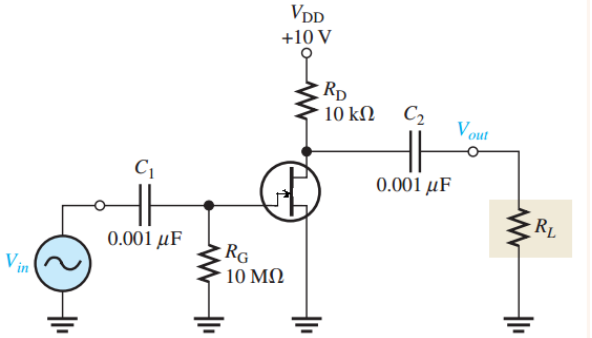

Figure 3